Advanced Heterogeneous Solutions for System Integration

Kees Joosse
Director Sales, Israel
TSMC
High-Growth Applications Drive Product and Technology

- Smartphone: 20%
- Cloud Data Center: 24%
- IoT: 30%

Source: TSMC Estimation; Gartner Research

CAGR 12’ – 17’
# High-End Smartphone

<table>
<thead>
<tr>
<th>Feature</th>
<th>2013</th>
<th>2015</th>
<th>2017</th>
</tr>
</thead>
<tbody>
<tr>
<td>LTE Spec</td>
<td>4G Cat.4</td>
<td>4G Cat.6</td>
<td>4G Cat.10</td>
</tr>
<tr>
<td>CPU</td>
<td>32bit Quad-Core</td>
<td>64bit Octa-Core</td>
<td>64bit Octa-Core</td>
</tr>
<tr>
<td>Video</td>
<td>H.264 1080p</td>
<td>H.265 2K</td>
<td>H.265 4K</td>
</tr>
<tr>
<td>Camera</td>
<td>13MP</td>
<td>24MP</td>
<td>32MP</td>
</tr>
<tr>
<td>Display</td>
<td>720p</td>
<td>1080p</td>
<td>4K</td>
</tr>
<tr>
<td>Battery</td>
<td>2600mAh</td>
<td>3000mAh</td>
<td>3200mAh</td>
</tr>
</tbody>
</table>

*Source: TSMC Estimation*
Cloud Data Center

<table>
<thead>
<tr>
<th></th>
<th>2013</th>
<th>2015</th>
<th>2017</th>
</tr>
</thead>
<tbody>
<tr>
<td>Connected Devices</td>
<td>7B</td>
<td>8B</td>
<td>9B</td>
</tr>
<tr>
<td>Data Traffic</td>
<td>1.6 Zettabyte</td>
<td>3.1 Zettabyte</td>
<td>5.1 Zettabyte</td>
</tr>
<tr>
<td>CPU</td>
<td>4~8 cores</td>
<td>8~18 cores</td>
<td>16~32 cores</td>
</tr>
<tr>
<td>Ethernet</td>
<td>10G</td>
<td>25/40G</td>
<td>40/100G</td>
</tr>
<tr>
<td>Storage</td>
<td>2 Exabyte</td>
<td>7 Exabyte</td>
<td>14 Exabyte</td>
</tr>
<tr>
<td>Power Budget</td>
<td>Same</td>
<td>Same</td>
<td>Same</td>
</tr>
</tbody>
</table>

Source: Cisco VNI 2014
Zetta:$10^{21}$; Exa: $10^{18}$
# Internet of Things: Wearables

<table>
<thead>
<tr>
<th></th>
<th>2015</th>
<th>2017</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>CPU</strong></td>
<td>32 bit / Dual Cores</td>
<td>64 bit / Dual Cores</td>
</tr>
<tr>
<td><strong>Clock speed</strong></td>
<td>1 -1.2GHz</td>
<td>1.2-1.5 GHz</td>
</tr>
<tr>
<td><strong>Connectivity</strong></td>
<td>802.11n, BT 4.0</td>
<td>802.11n/ac, BT 4.x</td>
</tr>
<tr>
<td><strong>Packaging</strong></td>
<td>SiP</td>
<td>SiP/ InFO</td>
</tr>
<tr>
<td><strong>Battery life</strong></td>
<td>1 Days</td>
<td>3~7 Days</td>
</tr>
</tbody>
</table>

*Source: TSMC Estimation*
Internet of Things is a Natural Extension of Mobile Computing

**Smart Wearables**
- Smart Watches, Smart Glasses, Fitness/Health Band, Smart Clothes.

**Smart Car**
- Collision Avoidance, Autonomous Driving, Infotainment.

**Smart Home**
- Smart Meter, Smart Appliance, Smart Lighting

**Smart City**
- Smart Parking, Smart Agriculture, Smart Water, Smart Grid, Smart Medical
IoT Product Requirements

- Smart Wearables
- Smart Home
- Smart Car
- Smart City

- "Right" Performance
- Compact Form Factor
- Lowest Power
- Integrated Functionality
- Cost Effective
- Tighter Security
IoT = Internet of Things

- Integrated Specialty Technology
- Ultra Low Power
- Advanced Packaging

IoT = Integration of Technologies
Energy Efficient System Scaling

Low Power CMOS - Moore’s Law

3D-IC Technology

Integrated Specialty Technology

- GAA- NWT
- III-V on Si CMOS
- Ge FinFET on Si
- TFET
- FinFET
- InFO
- CoWoS™ Si Interposer
- Cu-TSV Vertical Stacking

- Analog
- Mixed Signal
- BCD - Power IC
- BSI CIS
- CMOS MEMS
- HV
- eFlash

Open Innovation Platform®

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TSMC Integrated Specialty Technology

TSMC Ultra Low Power Platform
3D-IC technology and Heterogeneous Integration
TSMC WLSI Technology Platforms

- CoWoS: High performance and SoC partition
  - Very high memory bandwidth
  - Very wide envelope

- InFO: Multi-chips integration
  - Smallest form-factor
  - Cost competitive
What is InFO (=Integrated Fan Out)?

- **Single-Die InFO**: An extension of “Fan-in” WLCSP to enable more IOs

![Diagram of WLCSP to InFO]

- **Multi-Die InFO**: A solution for homogenous/heterogeneous integration in a single package

![Diagram of Multi-Die InFO]
CoWoS Technology

- Integrate multiple chips into one single package using a sub-micron scale silicon interface (interposer)

- Enable higher performance, lower power consumption, and smaller form factor

- Best integrated flow for high yield and reliability
**InFO/CoWoS® Portfolio**

**Small**
- Configuration: InFO + Inductor
- Applications: RF, WiFi
- Ball pitch: 0.4mm

**Large**
- Configuration: Multi dice, PoP supported
- Applications: AP, BB, FPGA
- RDL layer/pitch: 2/(2/2µm)
- Ball pitch: 0.4mm

**Super Large**
- Configuration: Multi dice
- Applications: AP, BB, GPU, FPGA, Networking
- RDL layer/pitch: 3/(2/2µm)
- Ball pitch: 0.4~1mm

**CoWoS®**
- Configuration: Multi dice
- Applications: GPU, FPGA, Networking
- RDL layer/pitch: 3 / (0.4/0.4µm)
- Ball pitch: 1mm

**InFO/CoWoS® Portfolio**

**Configuration**
- Multi dice

**Applications**
- AP, BB, FPGA
- GPU, FPGA, Networking

**RDL layer/pitch**
- 2/(2/2µm)
- 3/(2/2µm)
- 3 / (0.4/0.4µm)

**Ball pitch**
- 0.4mm
- 0.4~1mm
- 1mm

**InFO-HP (w/substrate)**

**InFO-LS**

**InFO-HP**

**Logic-1**

**Logic-2**

**InFO-LS**

**Package Size (mm)**

- 2x2
- 4x4
- 8x8
- 15x15
- 25x30
- 40x40
- 60x60

**I/O Count**

- 300
- 600
- 900
- 1200
- 1500

**InFO/CoWoS® Portfolio**

**Logic**
- 2
- 1

**InFO-LS**

**Open Innovation Platform®**

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InFO PoP 3D-Stacking

DRAM
InFO with TIV
CoWoS® Roadmap

CoWoS® (≤ 1 reticle size)
- C4 EU bump 180um pitch
- Substrate size 45x45mm²
- HD MiM (16 fF/um²)

CoWoS®-XL (> 1 reticle size)
- C4 Cu bump 180um pitch
- Substrate size 55x55mm²
- 4-height HBM
- Substrate size 60x60mm²
- C4 Cu bump 150um pitch
- 8-height HBM

Available Services

<table>
<thead>
<tr>
<th>Year</th>
<th>‘15</th>
<th>‘16</th>
<th>‘17</th>
</tr>
</thead>
</table>

- Left edge of each box represents package qual completion schedule
CoWoS® HBM Integration

- Successfully demonstrated integration of HBM in CoWoS® process with high uBump joint yield (>95%)
Interposer CoWoS® Integration
CoWoS® in Production

- Starting delivering CoWoS® product modules since 2012 on and at >96% production yield
- Customer successfully qualified both homogeneous and heterogeneous integration schemes
- Multiple customer design-ins

Homogeneous Integration in organic substrate (courtesy of Xilinx)

Heterogeneous Integration in ceramic substrate (courtesy of Xilinx)
3DIC TSV Status

- Technology features
  - Via-middle TSV process technology
  - Support face-to-back die stacking scheme (F/S flip chip bump + B/S μbump)
- Successfully passed process Qualification on N40 and N28HPM nodes
Summary

- Deliver right technology at right time to unleash your innovations and speed your time-to-market
  - Accelerate the pace of new technology roll out for high-performance products
  - Continue to invest in more cost-effective technology for mainstream products
  - Offer ultra-low power technologies for IoT and wearables markets

- Provide the most comprehensive design ecosystem to speed your design success