Foundry ESD Tool-set; from ESD Qualification Vehicle to ESD PDK and ESD Checkers

Efraim Aharoni, Roda Kanawati, Israel Rotstein, Avi Parvin, Hafez Khmaisy, Nissim Cohen

TowerJazz
Outline

• ESD Tool-Set Objective
• ESD Motivation - Reminder
• Foundry ESD Tool-Set – Introduction
• ESD/LU Qualification
• ESD PDK
• ESD Checkers
• Summary
ESD Tool-Set Objective

• In addition to the IO cells libraries, foundries offers a variety of tools supporting design for ESD protection.

• The ESD tool-set is crucial of course for the creation of the IO library, but it also enables ESD design by customers, especially when special requirements or specifications are not covered by the existing IO cells.

• Automatic tools for ESD checking, can increase the probability of ESD design success and short time to market.
ESD Motivation - Reminder

• On-chip ESD Protection (at IC level), should provide protection to the IC from ESD discharge during IC handling, packaging, and use

• Main ESD models/ratings (at wafer level)
  – Human Body Model (HBM) / 2000V
  – Machine Model (MM) / 200V
  – Charge Device Model / 500V

• Well-known Specifications for ESD models and tests
  – JEDEC, ESDA, AIC

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ESD Protection Requirements

- Clamp the ESD voltage to shunt the ESD stress current
- Turn on fast (less than 1ns)
- Carry large currents of ~2 A or more for ~150ns
- Have low on-resistance
- Occupy minimum area at bond pad
- Have minimum capacitance and series resistance
- Immune to process drifts
- Robust for numerous pulses
- Offer protection for various ESD stress models
- Not interfere with the IC functionality
- Not cause increased Vcc or IO leakage
- Survive the burn-in tests
Foundry ESD Tool-Set - Introduction

I/O cells
- ESD protected
- Guidance
- Placement

Design Rules
- Layout
- Electrical

PDK
- Devices pcells
- Cells

Guidance
- Schemes
- Simulations

Data for ESD Window
- ESD devices TLP
- Non-ESD

Checking tools
- ‘Run-sets’
- Checkers

ESD/LU Qualification Method

ESD Design Manual (EDM) and Process Design Kit (PDK)

Not replacing IO cells, but complementary

Covering all foundry flavors; Logic, analog, NVM, RF, PM, CIS...

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ESD/LU Qualification Vehicle

• Motivation
  – ESD/LU-related qualifications utilizing simple TEG. No need to base on product or IO library TEG
  – Examples: New technology, optical shrink, changing starting material, changing test specification (like automotive), etc.
  – The qualification results can be shared with customers

• Features
  – Protection circuits based on the foundry ESD protection guidance and ESD devices, with their special rules
  – Typical pins, representing IC pins; Input, Output, supplies. Power domain
  – Relevant non-ESD devices and circuits representing protected core

• Stress/Test
  – Following ESD/LU bench-mark specifications (JEDEC, ESDA, AIC)
  – Leakages checked before and after zap/stress
ESD/LU Qualification Vehicle – Circuit

Power clamp, 2 domains and back-to-back ESD diodes

Power clamp, Input with primary/secondary protection

Internal circuit
**ESD/LU Qualification Vehicle – Final Test**

- Example of leakage current results before and after ESD/LU test on J750 tester.
- Leakages measured at room-temperature and at 150°C, for automotive technology qualification.
- These results and the technology qualification report are shared with customers (in the technology qualification report)!

### TJP_3.3V TS18SL ESD and Latch-up Automotive test results

<table>
<thead>
<tr>
<th></th>
<th>Before ZAP</th>
<th>After ZAP</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>VDD-LKG (3.7V)</td>
<td>IO-LKG (3.7V)</td>
</tr>
<tr>
<td></td>
<td>IO=0V; VSS=GND</td>
<td>VDD=3.7V; VSS=GND</td>
</tr>
<tr>
<td></td>
<td>RT [pA]</td>
<td>150C [nA]</td>
</tr>
<tr>
<td>Presto Package #</td>
<td>2kV HBM</td>
<td>200V MM</td>
</tr>
<tr>
<td>Tower Package #</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>9</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>8</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>7</td>
<td>6</td>
<td>6</td>
</tr>
<tr>
<td>18</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>17</td>
<td>9</td>
<td>9</td>
</tr>
<tr>
<td>16</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>15</td>
<td>11</td>
<td>11</td>
</tr>
<tr>
<td>14</td>
<td>12</td>
<td>12</td>
</tr>
<tr>
<td>13</td>
<td>13</td>
<td>13</td>
</tr>
</tbody>
</table>

|                  | VDD-LKG (3.7V)      | IO-LKG (3.7V)       |
|                  | IO=0V; VSS=GND      | VDD=3.7V; VSS=GND   |
|                  | RT [pA]             | 150C [nA]           |
| Presto Package # | 2kV HBM             | 200V MM             |
| Tower Package #  |                     |                     |
| 1                | 1                   | 2                   |
| 2                | 2                   | 2                   |
| 3                | 3                   | 3                   |
| 9                | 4                   | 4                   |
| 8                | 5                   | 5                   |
| 7                | 6                   | 6                   |
| 18               | 8                   | 8                   |
| 17               | 9                   | 9                   |
| 16               | 10                  | 10                  |
| 15               | 11                  | 11                  |
| 14               | 12                  | 12                  |
| 13               | 13                  | 13                  |

**Example:**

- Example of leakage current results before and after ESD/LU test on J750 tester.
- Leakages measured at room-temperature and at 150°C, for automotive technology qualification.
- These results and the technology qualification report are shared with customers (in the technology qualification report)!
ESD DESIGN MANUAL AND PDK
ESD Design Manual

• ESD Models Overview and ESD/LU test references
• Information on special layers and masks for ESD (for LVS/DRC, ESD implant)
• ESD devices
  – Description of devices
  – Pcell information: names, parameters, limits, terminals, sub-circuits
  – ESD devices layout and electrical rules (per device)
  – General ESD rules
  – General Latch-Up rules
  – TLP characterization of ESD devices
• ESD protection circuits (schemes) guidelines
• Complementary TLP based data for ESD design window
  – Breakdown voltages of non-ESD (core) devices
  – Maximum current densities of interconnects
• RC Rail Clamp ESD Protection detailed guidelines, including simulation examples
ESD PDK

• Variety of ESD devices pcells (symbol, layout)
  – ESD multi-finger coupling diodes with TLP based SPICE models (required for RC Rail Clamp simulation)
  – ESD Transistors for IO, for power-clamp, pass-gate, over-voltage tolerant (OVT) cascade transistors
  – ESD transistors for Large Drivers. Special ESD layout rules → significant area reduction, optimized Rdson and LU robustness

• All pcells are DRC clean and Si proven
• ESD performance calculators (in some of the pcells)
• Accurate simulation at scheme stage.
• Devices symbols represent actual sub-circuit
  – Simple and natural implementation in circuits
  – Direct generation of appropriate layout
ESD PDK

- Pcells information is given in the EDM
  - Pcells parameters (some calculated) and limits, spice/LVS/PDK names, description of sub-circuit, Layers, terminals
  - Layout rules (per device)
  - Electrical rules
  - Required circuit for implementation of the device (sub-circuit)
    The sub-circuit is built-in to the layout generation
- GUI layout parameters for layout convenience and ESD performance
  - Number of source/drain metal layers
  - Number of last-metal layers (connected in parallel)
  - Poly gate routing options, etc.
List of the ESD Devices (pcells)

• NMOS/PMOS ESD Transistors for IO (salicide block on drain)
  – All fingers active, Active and dummy fingers
  – NMOS/PMOS Large Drivers (reduced area), for lower Rdson. Optimized trade-off of ESD performance vs. LU robustness.

• NMOS ESD Transistors for GCNMOS Power-Clamp circuit (NS on both source and drain)

• NMOS/PMOS ESD Pass-gate transistors (separate bulk terminal → No parasitic diode → Snapback in both polarities → Symmetrical salicide block on both diffusions).
  – All fingers active, Active and dummy fingers
List of the ESD Devices (pcells)

- Cascaded NMOS/PMOS ESD Transistors for Over-Voltage-Tolerant IO (in the same active) and Power Clamp
- ESD coupling diodes
  - TLP-based SPICE models for RC Rail-Clamp simulation
  - RF Models for RF design
- Special supporting devices (non-snapback)
  - NMOS/PMOS transistors for boosted RC Rail Clamp (SPICE models above Vdd)
- ESD devices for POWER MANAGEMENT (up to 700V)
  - Scalable ESD devices (voltage, ESD rating)
  - Variety of voltage platforms
  - For both snapback and RC Rail Clamp protection
ESD Devices – Electrical and Layout Rules (Example)

Design Rules of 3.3V ESD Transistor for I/O:

<table>
<thead>
<tr>
<th>Rule name</th>
<th>Rule description</th>
<th>Action</th>
<th>Drawn</th>
</tr>
</thead>
<tbody>
<tr>
<td>N33_ESD.W.1</td>
<td>Gate length of 3.3V nMOS transistor</td>
<td>min</td>
<td>0.4</td>
</tr>
<tr>
<td>N33_ESD.W.2</td>
<td>Gate length of 3.3V nMOS transistor</td>
<td>max</td>
<td>0.5</td>
</tr>
<tr>
<td>N33_ESD.L</td>
<td>Total W. This rule is NOT checked by DRC</td>
<td>min</td>
<td>360</td>
</tr>
<tr>
<td>N33_ESD.F0</td>
<td>NS width on Drain AA (related only to parallel to gate fingers direction toward AA edge)</td>
<td>min</td>
<td>1.95</td>
</tr>
<tr>
<td>N33_ESD.F1</td>
<td>NS width on Drain AA (related only to perpendicular to gate fingers direction)</td>
<td>min</td>
<td>3</td>
</tr>
<tr>
<td>N33_ESD.O</td>
<td>Overlap of NS with GC Gate</td>
<td>exact</td>
<td>0.05</td>
</tr>
<tr>
<td>N33_ESD.D</td>
<td>Distance from Source CS to GC Gate</td>
<td>min</td>
<td>0.75</td>
</tr>
</tbody>
</table>

Electrical rules, not checked by DRC: Total W ≥ 360µm

Even number of gate fingers

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<table>
<thead>
<tr>
<th>ESD Transistor</th>
<th>Spice name</th>
<th>LVS name</th>
<th>PDK name</th>
<th>PDK Sub-Circuit</th>
<th>Recognition layers, Terminals, and Parameters</th>
<th>Spice terminals and parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cascaded 3.3V NMOS ESD Transistors for 5V OVT I/O PAD, only part of the fingers are Active and the rest are dummy</td>
<td>nhv</td>
<td>n335acasesd</td>
<td>casesdn335</td>
<td><img src="image.png" alt="Diagram" /></td>
<td>Drawn layers: AA, GC, XN, AREA2, ESD5OVT(lc), AA(ed), DEV_AREA(ed), AREA10(ed) Terminals: S, G1, G2, D, B. Parameters: w, l, nf, nfa</td>
<td>Terminals: D, G, S, (B=S) Parameters: w, l, m, ad, as, pd, ps</td>
</tr>
</tbody>
</table>

| Cascade 3.3V NMOS ESD Transistor for 5V OVT of Power Clamp or for Vpp of Input only | nhv        | n335pccasesd  | casesdn33pc5     | ![Diagram](image.png) | Drawn Layers: AA, GC, XN, AREA2, ESD5OVT(lc), ESD5OVT(kt), AA(ed), DEV_AREA(ed), DEV_AREA(cs), AREA10(ed) Terminals: S, G1, G2, D, B. Parameters: w, l, nf | Name: nhv Terminals: D, G, S, (B=S) Parameters: w, l, m, ad, as, pd, ps, |
ESD pcells Examples – Symbols

5V NMOS ESD Transistors for I/O (all fingers are active)

5V NMOS ESD Transistors for I/O, active and dummy fingers \((W_A + W_D \geq 360 \mu m)\)
ESD pcells Examples – Symbols

5V NMOS ESD Pass gate Transistor (active and dummy fingers)
Cascaded 3.3V ESD Transistors for 5V OVT IO, active and dummy fingers. Both gates are in the same active area.

nfa – number of active fingers
nf - number of fingers (nf=nfa + nfd)

w – total width
w=w_a+w_d
ESD pcell GUI Example

nfa – number of active fingers
nf - number of fingers
(nf=nfa + nfd)

w – total width
w=w_a+w_d

Prevents electrical rule violation (W<min is not aloud, parameters out of limits not aloud, default parameters)

Actual average diffusion dimensions (area, perimeter) are calculated based on device parameter (finger width, number of fingers) → Extracted and used in SPICE model
# pCell Callback - Examples

ESD Transistor (all fingers active)
vs. non-ESD transistor

ESD Transistor (active and dummy gate fingers)

<table>
<thead>
<tr>
<th>param.</th>
<th>units</th>
<th>n33</th>
<th>esdn33a</th>
</tr>
</thead>
<tbody>
<tr>
<td>ad</td>
<td>µm²</td>
<td>12.2</td>
<td>149.9</td>
</tr>
<tr>
<td>as</td>
<td>µm²</td>
<td>14.5</td>
<td>42.2</td>
</tr>
<tr>
<td>pd</td>
<td>µm</td>
<td>45.5</td>
<td>51.7</td>
</tr>
<tr>
<td>ps</td>
<td>µm</td>
<td>64.5</td>
<td>58.1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>gate</th>
<th>param.</th>
<th>units</th>
<th>esdn33</th>
</tr>
</thead>
<tbody>
<tr>
<td>active</td>
<td>ad</td>
<td>µm²</td>
<td>149.9</td>
</tr>
<tr>
<td>active</td>
<td>as</td>
<td>µm²</td>
<td>45.7</td>
</tr>
<tr>
<td>active</td>
<td>pd</td>
<td>µm</td>
<td>51.7</td>
</tr>
<tr>
<td>active</td>
<td>ps</td>
<td>µm</td>
<td>69.6</td>
</tr>
<tr>
<td>dummy</td>
<td>ad</td>
<td>µm²</td>
<td>149.9</td>
</tr>
<tr>
<td>dummy</td>
<td>as</td>
<td>µm²</td>
<td>41</td>
</tr>
<tr>
<td>dummy</td>
<td>pd</td>
<td>µm</td>
<td>51.7</td>
</tr>
<tr>
<td>dummy</td>
<td>ps</td>
<td>µm</td>
<td>54.3</td>
</tr>
</tbody>
</table>
Casesdn555 (Cascade of 3.3V ESD transistors for 5V OVT, active and dummy gate fingers)

<table>
<thead>
<tr>
<th>gate</th>
<th>param.</th>
<th>units</th>
</tr>
</thead>
<tbody>
<tr>
<td>G1 active</td>
<td>ad</td>
<td>µm²</td>
</tr>
<tr>
<td>G1 active</td>
<td>as</td>
<td>µm²</td>
</tr>
<tr>
<td>G1 active</td>
<td>pd</td>
<td>µm</td>
</tr>
<tr>
<td>G1 active</td>
<td>ps</td>
<td>µm</td>
</tr>
<tr>
<td>G1 dummy</td>
<td>ad</td>
<td>µm²</td>
</tr>
<tr>
<td>G1 dummy</td>
<td>as</td>
<td>µm²</td>
</tr>
<tr>
<td>G1 dummy</td>
<td>pd</td>
<td>µm</td>
</tr>
<tr>
<td>G1 dummy</td>
<td>ps</td>
<td>µm</td>
</tr>
<tr>
<td>G2 active</td>
<td>ad</td>
<td>µm²</td>
</tr>
<tr>
<td>G2 active</td>
<td>as</td>
<td>µm²</td>
</tr>
<tr>
<td>G2 active</td>
<td>pd</td>
<td>µm</td>
</tr>
<tr>
<td>G2 active</td>
<td>ps</td>
<td>µm</td>
</tr>
<tr>
<td>G2 dummy</td>
<td>ad</td>
<td>µm²</td>
</tr>
<tr>
<td>G2 dummy</td>
<td>as</td>
<td>µm²</td>
</tr>
<tr>
<td>G2 dummy</td>
<td>pd</td>
<td>µm</td>
</tr>
<tr>
<td>G2 dummy</td>
<td>ps</td>
<td>µm</td>
</tr>
</tbody>
</table>
ESD Protection Circuit Guidance – Schemes

• Design guidance for both normal operation and ESD protection
• Output (self-protected)
• Input or I/O (bidirectional input/output)
  – All gate fingers active
  – Active and dummy gate fingers
  – Negative input
• Power Clamp
• Over-Voltage-Tolerant pins; input, I/O, power clamp
• Full IC; I/O ring, busses, multiple domains
Example – Protection Scheme for I/O Protection

Scheme of I/O CMOS buffer with complementary dummy finger transistors:
M3 & M5 represent active and dummy gate fingers, in one NMOS ESD transistor for I/O device (one pcell with 2 gate terminals).
M4 & M6 – Active and dummy gates of PMOS ESD transistor For I/O (one pcell)
M7 – ESD trans. For power-clamp, part of GCMOS power-clamp cell
M1 & M2 – Soft pull-down/pull-up of dummy gates, during normal operation.
M8 & M9 – Secondary transistors.

M3/M5, M4/M6, and M7 are ESD devices pcells!
RC Rail Clamp Protection Guidelines

- ESD protection circuit is not based on snapback devices.
  - ESD protection design is based on SPICE simulation → predictable results
  - Low capacitive load on input pins (for RF design)

- The guidance contains
  - Schematic description of the protection circuits and components
  - Analysis of ESD paths and voltage clamping of core
  - Circuits used for generation of HBM and MM waveforms
  - Step by step simulation guidance, to ensure voltage clamping

- ‘Boosted’ bigFET’ with special SPICE models
  - SPICE models support Vgs>Vdd
  - Enables bigFET current over-drive and significant area reduction

- Guidance for different specifications
  - High ESD rating
  - Negative input
  - Over-voltage tolerant I/O’s

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RC Rail Clamp Protection Simulations

HBM/MM ESD pulse generators, used to create ESD current waveforms, for SPICE simulations. ESD rating is defined by the voltage pulse

![Diagrams and waveforms showing ESD current waveforms for HBM/MM ESD pulse generators.]

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**Figure 10-7:** Simulation of voltage drop across the NMOS bigFET during ESD zap. (a) First 2 ns of ESD zap. (b) 200 ns after zap start.
ESD Characterization

- ESD characterization data is required for appropriate ESD protection design, obeying safe ‘ESD protection design window’
  - Ensure ESD protection device off and no Latch-Up risk during IC normal operation
  - Ensure conductance of ESD current and voltage clamping of protected circuit, during the ESD event (both polarities)
- Type of data
  - ESD characterization is based on Transmission Line Pulse (TLP) measurements
  - DC I-V to check leakage at normal operation
- Required characterization
  - Critical parameters of ESD devices (Vt1/Von, Vh, Vt2, it2, Ron)
  - Breakdown voltages of non-ESD devices (to be protected)
  - Max ESD current densities and resistances of interconnects (to carry the ESD current)
ESD Transistor for Power Clamp - TLP Characterization

Measurement set-up:

TLP pos. zap at various Vgs biases:

Vgs=0.6V

Vgs=0

<table>
<thead>
<tr>
<th></th>
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<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>6</td>
<td>4.44</td>
<td>5.23</td>
<td>1.63</td>
<td>0.651</td>
</tr>
<tr>
<td>0.2</td>
<td>5.89</td>
<td>4.45</td>
<td>5.29</td>
<td>1.63</td>
<td>0.663</td>
</tr>
<tr>
<td>0.35</td>
<td>5.7</td>
<td>4.39</td>
<td>5.48</td>
<td>1.55</td>
<td>0.8</td>
</tr>
<tr>
<td>0.4</td>
<td>5.28</td>
<td>4.29</td>
<td>5.09</td>
<td>1.55</td>
<td>0.688</td>
</tr>
<tr>
<td>0.5</td>
<td>4.56</td>
<td>4.2</td>
<td>5.43</td>
<td>1.8</td>
<td>0.654</td>
</tr>
<tr>
<td>0.55</td>
<td>4.26</td>
<td>4.11</td>
<td>5.18</td>
<td>1.82</td>
<td>0.552</td>
</tr>
<tr>
<td>0.6</td>
<td>4.25</td>
<td>4.12</td>
<td>5.34</td>
<td>1.69</td>
<td>0.493</td>
</tr>
<tr>
<td>0.75</td>
<td>4.1</td>
<td>4.1</td>
<td>5.38</td>
<td>1.88</td>
<td>0.67</td>
</tr>
</tbody>
</table>
Use of Characterization Data (Example)

- This scheme representing ‘open-drain’ ESD protection circuit, used in VerilogA simulation.
- The ‘bipolar transistor’ is a representation of a piecewise linear model of the TLP curve.
- The actual reduction of $V_{t1}$ due to jump of $V_{gs}$ is taken into account by combining with the regular SPICE simulation.

![IV Chart](image)

$V_{DUT}$ (V) vs. $I_{DUT}$ (A)

$R_{pcp}=0$

$E_{SD}$ (A) vs. $V_{ESD}$ (V)
Use of Characterization Data (Example)

2KV HBM – VDD to PAD

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Use of Characterization Data (Example)

MM – VDD to Vss
ESD CHECKERS
# ESD Checking - Overview

- **Automatic** verification of ESD robustness of Integrated Circuits is an emerging part of the design review procedure and design flow
- **DRC** is layout-based (and not scheme-based), can be used only close to tape-out, and does not verify ESD path
- Existing and developed checks can be categorized as either Design-Rule check or Robustness check;

<table>
<thead>
<tr>
<th>Item</th>
<th>Check</th>
<th>Challenge/Comment</th>
<th>PDK benefit</th>
</tr>
</thead>
<tbody>
<tr>
<td>ESD dedicated layout rules</td>
<td>DRC (Design Rule Check)</td>
<td>Accurate layers placement (some for DRC purpose only)</td>
<td>Pcells are ‘DRC clean’</td>
</tr>
<tr>
<td>ESD electronic rules</td>
<td>ERC (Electronic Rule Check)</td>
<td>Need to ‘translate’ guidelines and schemes to code</td>
<td>Pcells are ‘ERC clean’</td>
</tr>
<tr>
<td>ESD path verification</td>
<td>Existence of ESD path</td>
<td>Recognition of ESD devices</td>
<td>Simple identification of ESD devices</td>
</tr>
<tr>
<td>Voltage Clamping</td>
<td>Static</td>
<td>ESD device modeling? Dynamic check?</td>
<td>TLP characterization</td>
</tr>
<tr>
<td></td>
<td>Dynamic</td>
<td>Huge data-base is required</td>
<td></td>
</tr>
<tr>
<td>Current density, along ESD path</td>
<td>Point to point</td>
<td>Used also for EM robustness check</td>
<td>TLP characterization (of interconnects)</td>
</tr>
</tbody>
</table>
Approaches of Implementing PERC in TowerJazz*

Pre layout
- Topological checking with schematic

Post layout
- Schematic info. driven geometrical check

Design rules manual
- ESD design guidelines

Implement key items from design rules and ESD design guidelines to PERC that traditional tools cannot check automatically

May 6, 2015
PERC Implementation: ESD IO Rules

Target:

Transistor connected directly by its drain to IO and source to power rail is considered as an ESD transistor and hence must comply with ESD design rules.
PERC Implementation Example: ESD IO Rules

- **Topological checking**
  - Width/Length uniformity check
  - Length check comparing to recommend value
  - Total width check for same MOS gate fingers
  - Soft Vdd/Vss transistor check for the dummy NMOS/PMOS

- **Geometrical checking**
  - All Gate Fingers of the same MOS should be placed in the same active rectangular polygon in order to ensure full triggering matching between all gate fingers during ESD event
  - Number of gate fingers should be even
  - Source side should be placed at the two edges of the AA
Topological Checking Example of ESD IO Rules

Error detected due to “Missing soft Vdd transistor for the dummy NMOS”
ESD OFFERING FOR POWER MANAGEMENT PLATFORMS (JUST TASTE)
ESD Challenges:
1. Good Vdd Rdson Tradeoff \((BVdss-ESD \text{ design window} = Vdd)\)
2. Scalable voltage platform \(\Rightarrow\) Need scalable ESD voltage solutions
3. Capability to tune ESD Rating.
4. Small footprint.

Current

Voltage

Thermal Failure Effect

IC operation area

Safe ESD protection window

Min Breakdown/Rel. Voltage of IC due to ESD transient on TLP pulse

Safety margin

(Vt2, It2)

(Vt1, It1)

Vdd

Voltage

ChipEx 2015

May 6, 2015
If the 5V GND and the HV GND have the same potential, then this rail protection could be replaced by 5V anti parallel ESD coupling diodes.
TS18PM/TS35PM ESD protection devices comparison

<table>
<thead>
<tr>
<th></th>
<th>CGNLDMos</th>
<th>SCR</th>
<th>PNP</th>
<th>NPN¹</th>
</tr>
</thead>
<tbody>
<tr>
<td>Scalable voltage</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Scalable ESD ratings</td>
<td>✓</td>
<td>✓</td>
<td>X</td>
<td>✓</td>
</tr>
<tr>
<td>Predictable ESD performance, using normal operation Spice model</td>
<td>✓</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>High immunity to false triggering</td>
<td>X</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>High holding voltage</td>
<td>NA</td>
<td>X</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Clamp size for 40V application 2KV-HBM &amp; 200V-MM</td>
<td>~44,000 μm²</td>
<td>~1400 μm²</td>
<td>~55,000 μm²</td>
<td>~10,800μm²</td>
</tr>
</tbody>
</table>

¹ Available only for Shallow NBL Platform
Summary

• TowerJazz rich ESD PDK enables design ease and higher probability of IC ESD protection safe time success.

• Based on long interaction with our customers and evaluation of designers needs, TowerJazz developed a long list of devices and protection schemes covering a wide range of IC pins and specifications.

• Automatic tools are continuously adopted for ESD Electronic rules check. TowerJazz implemented Calibre PERC and plans additional tools to cover other aspects of ESD protection verification.

• TowerJazz offers a full ESD coverage for PM platforms including:
  - Scalable voltage ESD solutions
  - Scalable ESD rating solutions
  - Both RC coupled and voltage triggered solutions
  - ESD pcells including ESD parameters calculators