High speed asynchronous serial link

Yongxin Zhang

Advisors: Ran Ginosar & Aharon Unikovski
Presentation Outline

• FOX2 Architecture
• FOX2 implementation
• Transmitter
  • Clock generator
  • Shift register
  • LEDR encoder
  • Analog Transmitter
• Transmission line
• Receiver
  • Analog Receiver
  • Splitter
  • Shift register
• Integration of TX and RX
• Transition signaling
  – two-phase NRZ
  – Level Encoded Dual Rail (LEDR)
  – asynchronous protocol, a.k.a. data-strobe (DS)
• Wave-pipelining over channel
• Differential encoding (DS-DE, IEEE1355-95)
• Either current or voltage mode signaling
FOX2 implementation

- Target: 10Gbps over 10mm (FO4 - 11.3Gbps)
- Tower 0.18u, 1.8V
- Low number of metals → M6 transmission line
- EDA: Cadence Virtuoso

6M1L metal stack
Delay Element
Post layout simulation shows the maximum working frequency is around 12Gbps.
Post layout simulation shows the maximum working frequency to be 8.32 Gbps
• Transition Latch (XL)
  – Two separate data paths
  – controlled by differential signal C/CN
• Data of two data paths merged at the output stage of the SR
Post layout simulation shows the maximum working speed at around 8.4Gbps.
LED R Encoder

Uncoded (B) 0 0 1 1 0 0 0 0 1 0

Strobe bit (S) 

Data bit (D)

\[
S(i) = \begin{cases} 
\overline{B(i)}, & i \text{ odd} \\
B(i), & i \text{ even} 
\end{cases}
\]

\[
D(i) = B(i) \quad \forall i
\]
LEDRI Encoder

Maximum working speed around 11Gbps
Analog TX

High capacitance long interconnect restrains bandwidth, degrades signal.

CM lower swing, less power, longer distance, faster operation vs. VM

M11, M22 help to draw current at beginning of first toggle.

Current Mode TX

With Adaptive Control

May 6, 2015
Transmission line

Characteristic impedance $Z_0$ (model):
- $36.5 \Omega$ (h=0.82u)
- $77.8 \Omega$ (h=6.26u)

V,I at output $\sim$ proportional to $\Rightarrow \frac{R}{Z_0^x}$

$Z_0 \downarrow \Rightarrow$ attenuation↑, performance↓

Choose M6 as the line, M5 as the ground

Use RLC model for transmission line. Get $Z_0$. Use resistance $\sim$ size of line.

$\Rightarrow$ Find capacitance, inductance per unit length

\[
Z_0 = \sqrt{\frac{Z}{Y}} = \sqrt{\frac{R + j\omega L}{-j\omega C}}
\]
Transmission line

<table>
<thead>
<tr>
<th>type</th>
<th>T</th>
<th>H</th>
<th>W</th>
<th>Z0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Regular microstripe line with regular thickness and regular height</td>
<td>0.94</td>
<td>0.82</td>
<td>5</td>
<td>37.8</td>
</tr>
<tr>
<td>2. Regular microstripe line with regular thickness but higher height</td>
<td>0.94</td>
<td>6.26</td>
<td>5</td>
<td>76.2</td>
</tr>
<tr>
<td>3. Regular microstripe line with thicker thickness and regular height</td>
<td>2.3</td>
<td>0.82</td>
<td>5</td>
<td>32.8</td>
</tr>
<tr>
<td>4. Regular microstripe line with thicker thickness and higher height</td>
<td>2.3</td>
<td>4.9</td>
<td>5</td>
<td>66.9</td>
</tr>
<tr>
<td>5. U shape line with regular thickness and height</td>
<td>0.94</td>
<td>0.82</td>
<td>5</td>
<td>36.5</td>
</tr>
<tr>
<td>6. U shape line with regular thickness but higher height</td>
<td>0.94</td>
<td>6.26</td>
<td>5</td>
<td>77.8</td>
</tr>
<tr>
<td>7. U shape line with thick thickness and regular height</td>
<td>2.3</td>
<td>0.82</td>
<td>5</td>
<td>32.1</td>
</tr>
<tr>
<td>8. U shape line with regular thickness but not regular height</td>
<td>2.3</td>
<td>4.9</td>
<td>5</td>
<td>66.4</td>
</tr>
<tr>
<td>9. Line with shield, regular line and regular height</td>
<td>0.94</td>
<td>0.82</td>
<td>5</td>
<td>34.2</td>
</tr>
<tr>
<td>10. Line with shield, regular line and higher height</td>
<td>0.94</td>
<td>6.26</td>
<td>5</td>
<td>74.3</td>
</tr>
<tr>
<td>11. Line with shield, thick line and regular height</td>
<td>2.3</td>
<td>0.82</td>
<td>5</td>
<td>27.2</td>
</tr>
<tr>
<td>12. Line with shield, thick line and higher height</td>
<td>2.3</td>
<td>4.9</td>
<td>5</td>
<td>59.3</td>
</tr>
<tr>
<td>13. Coupled line with regular line and regular height</td>
<td>0.94</td>
<td>0.82</td>
<td>5</td>
<td>36</td>
</tr>
<tr>
<td>14. Coupled line with regular line and higher height</td>
<td>0.94</td>
<td>6.26</td>
<td>5</td>
<td>78.7</td>
</tr>
</tbody>
</table>

Same dimension ⇒ ~ same Z0 (seems the shape is not so important)
Transmission line

4 different configurations of the line:
regular thickness, regular height – a
regular thickness, higher height – b
thicker and regular height – c
thicker and higher – d
Analog RX  CG and RGC (Regulated-Cascaded) stage

Common gate trans-impedance commonly utilized for wide bandwidth (isolates large input capacitance)
Regulated-cascaded trans-impedance is more effective

\[ Z_{in1} = \frac{1}{g_{m1}} \]

Common gate

\[ Z_{in2} = \frac{1}{g_{m1}(1 + g_{mb}R_B)} \]

Regulated-cascaded
Analog RX

RGC TIA – Regulated-Cascoded Transimpedance Amplifier

M2 isolates large input capacitance of M3, changes signal DC voltage. But decreases open loop gain, influences linearity. Rf feedback helps bandwidth: dominant pole at drain(M1) rather than at input. Output DC point too low: need to drive digital circuit. Prefer 1/2 VDD.
Analog RX

RGC TIA – modification #1

Output stage: Source follower → common source (for higher output DC)
BUT: Gain too high, bandwidth too low (1GHz).
Eliminated last two stages
Faster, reasonable output DC level
Analog RX

Feedback limits frequency
-- loop has to close
-- requires high current
-- still, slower than open loop

Final Result: No feedback
Analog RX

Test bench, schematic, layout and performance

10mm Al line, $Z_0 = 36 \, \Omega$  $\rightarrow$  Max frequency 8.3Gbps
Advantages of differential amplifier:

Less sensitive to noise
Better common-mode noise rejection

Simulation: maximum frequency (10 mm Al line)
8.5 Gbps
– better than single ended
### Analog RX

**2T 2X config & Performance summary**

A simple voltage mode circuit:
- two inverters as analog TX
- two inverters as analog RX

![Circuit Diagram]

<table>
<thead>
<tr>
<th>link number</th>
<th>config</th>
<th>Fre/Gbps</th>
<th>Power/mA</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Z0a AL</td>
<td>8.6</td>
<td>5.178</td>
</tr>
<tr>
<td>2</td>
<td>Z0a 6A1</td>
<td>11.5</td>
<td>6.8</td>
</tr>
<tr>
<td>3</td>
<td>Z0a AL 2S</td>
<td>10.2</td>
<td>11.97</td>
</tr>
<tr>
<td>4</td>
<td>Z0b AL</td>
<td>12.9</td>
<td>3.526</td>
</tr>
<tr>
<td>5</td>
<td>Z0b 6AL</td>
<td>10.8</td>
<td>1.655</td>
</tr>
<tr>
<td>6</td>
<td>Noline</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>RGCTIA_Z0a_AL</td>
<td>8.3</td>
<td>20.8</td>
</tr>
<tr>
<td>8</td>
<td>RGCTIA_Z0a_6AL</td>
<td>9.8</td>
<td>21.5</td>
</tr>
<tr>
<td>9</td>
<td>RGCTIA_Z0b_AL</td>
<td>11.4</td>
<td>22.43</td>
</tr>
<tr>
<td>10</td>
<td>RGCTIA_Z0b_6AL</td>
<td>12.2</td>
<td>23.33</td>
</tr>
<tr>
<td>11</td>
<td>RGC TIA Noline</td>
<td>11.5</td>
<td>23.35</td>
</tr>
<tr>
<td>12</td>
<td>DFAM_Z0a_AL</td>
<td>8.5</td>
<td>24.16</td>
</tr>
<tr>
<td>13</td>
<td>DFAM_Z0a_6AL</td>
<td>9.8</td>
<td>24.72</td>
</tr>
<tr>
<td>14</td>
<td>DFAM_Z0b_AL</td>
<td>11.3</td>
<td>25.54</td>
</tr>
<tr>
<td>15</td>
<td>DFAM_Z0b_6AL</td>
<td>11.3</td>
<td>26.01</td>
</tr>
<tr>
<td>16</td>
<td>DFAM_Noline</td>
<td>11.3</td>
<td>25.98</td>
</tr>
<tr>
<td>17</td>
<td>Z0c AL</td>
<td>10.6</td>
<td>5.848</td>
</tr>
<tr>
<td>18</td>
<td>Z0c 6A1</td>
<td>12.4</td>
<td>7.482</td>
</tr>
<tr>
<td>19</td>
<td>Z0c AL 2S</td>
<td>11.4</td>
<td>13</td>
</tr>
<tr>
<td>20</td>
<td>Z0d AL</td>
<td>12.7</td>
<td>3.46</td>
</tr>
<tr>
<td>21</td>
<td>Z0d 6AL</td>
<td>10.8</td>
<td>1.655</td>
</tr>
<tr>
<td>22</td>
<td>RGCTIA_Z0c_AL</td>
<td>8.8</td>
<td>20.99</td>
</tr>
<tr>
<td>23</td>
<td>RGCTIA_Z0c_6AL</td>
<td>10.4</td>
<td>21.92</td>
</tr>
<tr>
<td>24</td>
<td>RGCTIA_Z0d_AL</td>
<td>11.3</td>
<td>22.42</td>
</tr>
<tr>
<td>25</td>
<td>RGCTIA_Z0d_6AL</td>
<td>12.2</td>
<td>23.23</td>
</tr>
<tr>
<td>26</td>
<td>DFAM_Z0c_AL</td>
<td>9.2</td>
<td>24.47</td>
</tr>
<tr>
<td>27</td>
<td>DFAM_Z0c_6AL</td>
<td>10.8</td>
<td>25.18</td>
</tr>
<tr>
<td>28</td>
<td>DFAM_Z0d_AL</td>
<td>10.8</td>
<td>24.45</td>
</tr>
<tr>
<td>29</td>
<td>DFAM_Z0d_6AL</td>
<td>11.3</td>
<td>25.83</td>
</tr>
<tr>
<td>30</td>
<td>AHCM</td>
<td>9.4</td>
<td>42.11</td>
</tr>
</tbody>
</table>
Toggle circuit – splitter
The maximum working frequency can be as much as 12.6 Gbps
Splitter
Post layout simulation shows the maximum working speed is around 8.6Gbps
Transition Latch (XL)

Two separate data paths controlled by differential signal C/CN

Data will be stored at the output of the SR after transition is finished
Post layout simulation shows the maximum working speed is around 8.1Gbps
TX integration

Add decoupling capacitors for power-supply consideration
RX integration

RX layout with decoupling capacitors
THANKS!!!