Zero-Defect Methodology for Automotive and Other Key Applications

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GUC Corporation Information

- Public company, traded in Taipei Stock Exchange
- Partially owned by TSMC
- Services: ASIC, Chip design service, IPs
- Worldwide offices: US, China, Europe, Japan and Korea
- Verisense, GUC Israeli partner, offers leading ASIC & FPGA design services
Automotive IC Reliability Requirements

- **Reliability: < 5 FIT**
  - FIT (failure in time) is defined as a failure rate of 1 per billion hours
  - 1 FIT is equivalent to having an MTBF of 1 billion hours

- **Defects < 5-10 DPPM**
  - DPPM: defective parts per million ppm

- **High max. ambient temperature**

<table>
<thead>
<tr>
<th>Grade</th>
<th>Operation Ambient Temperature</th>
<th>Min.</th>
<th>Max.</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>- 40 °C</td>
<td></td>
<td>150 °C</td>
</tr>
<tr>
<td>1</td>
<td>- 40 °C</td>
<td></td>
<td>125 °C</td>
</tr>
<tr>
<td>2</td>
<td>- 40 °C</td>
<td></td>
<td>105 °C</td>
</tr>
<tr>
<td>3</td>
<td>- 40 °C</td>
<td></td>
<td>85 °C</td>
</tr>
</tbody>
</table>
GUC Comprehensive Reliability Management

- Reliability control at all stages thought the flow

Design
- DFR Reliability
- DFM Manufacturing
- DFT Testing

Production
- Risk/Robustness checking
- ZD testing method
- Outlier program
- Tightened Control

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## Failures Distribution in Time

### Failures category

#### Main cause

- **Early failures**
  - Defect
  - Process Baseline
  - Product design

- **Random failures**
  - Defect
  - Process Baseline
  - Product design

- **Wear-out failures**
  - Defect
  - Process Baseline
  - Product design

#### Mechanism

- **Early failures**
  - High Test coverage
  - Outlier screening
  - 3-temp. testing
  - Visual spec. tighten
  - Burn-in testing

- **Random failures**
  - SPC/Cpk control
  - Equipment monitor
  - Reliability monitor
  - Continuous improvement

- **Wear-out failures**
  - Circuit design robustness
  - Design for Manufacturing
  - Package/material robustness
  - Drift analysis for spec margin

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# DFT Approach for Automotive Product

<table>
<thead>
<tr>
<th>DFT Item</th>
<th>Automotive product</th>
</tr>
</thead>
</table>
| **Digital** | • Stack at faults coverage > 99%  
• Transition faults coverage > 85%  
• Pseudo Stuck-at IDDQ faults coverage > 80%  
• Small Delay (Optional)  
• Bridge (Optional) |
| **SRAM** | • March 68N  
• Checkerboard & Inverse background data  
• Physical mapping |
| **ROM** | • ReadOnly 2N |
| **Analog** | • Functionality and Spec check  
• Additional signal to increase analog testability  
  - internal reference voltage monitor  
  - analog bias tuning setting to touch performance boundary  
• Analog test modes built in |
Silicon Process Variation

- Variation measured by Process Monitor (PM)
VMK: Variation Measurement Kit

- PMs inserted on regular grid
- PMs represent all used VTs, channel lengths, gates types
- Interface protocols: APB, JTAG, I²C
- Automatic test pattern generation
- Spice simulated in all corners for reference
- Statistic is collected through all wafers production
Soft Error Rate and Solution

• **Soft errors are induced by external radiation (e.g. alpha particles)**

• **Solutions**
  – Design: flip-flop
  – Memory: ECC
  – Package: low-alpha materials
DFM: Extended Physical Rules Check

- **Metal Thickness Variation**
  - Metal Filling
  - VCMP Thickness Hotspot

- **Lithography Pattern Failure**
  - Bridging
  - Metal Pinch
  - Hot-Spot

- **Via Voidance**
  - Double Via
  - Critical Area Fixing
DFM: Tightening Electromigration Rules

- **EM rating for automotive:**

<table>
<thead>
<tr>
<th>Temperature</th>
<th>100°C</th>
<th>105°C</th>
<th>110°C</th>
<th>115°C</th>
<th>120°C</th>
<th>125°C</th>
<th>130°C</th>
<th>140°C</th>
<th>150°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rating factor of Imax</td>
<td>2.077</td>
<td>1.434</td>
<td>1.000</td>
<td>0.704</td>
<td>0.500</td>
<td>0.358</td>
<td>0.258</td>
<td>0.138</td>
<td>0.076</td>
</tr>
</tbody>
</table>

  Figure: Rating factor for regular products

<table>
<thead>
<tr>
<th>Temperature</th>
<th>85°C</th>
<th>105°C</th>
<th>110°C</th>
<th>125°C</th>
<th>150°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rating factor of Imax</td>
<td>8.840</td>
<td>4.007</td>
<td>2.794</td>
<td>1.000</td>
<td>0.212</td>
</tr>
</tbody>
</table>

  Figure: Rating factor for automotive products

- **Additional Poly/High-R/Metal-gate R current density rule**

<table>
<thead>
<tr>
<th>Temperature</th>
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<th>105°C</th>
<th>110°C</th>
<th>125°C</th>
<th>150°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rating factor of Imax</td>
<td>1.24</td>
<td>1.11</td>
<td>1.08</td>
<td>1</td>
<td>0.89</td>
</tr>
</tbody>
</table>

  Figure: Poly EM requirement for regular products
Potential Defect Identification

- Production test tightening for Outliers segregation

![Diagram showing potential defect identification with upper and lower spec limits and tightening areas for outliers]
Outlier Program at Production Test

• **ELFR (Early Life Failure Rate)**
  – more than 2000 samples or production ramp-up, with HTOL method to identify the early failure mode/rate for CIP

• **Dynamic Voltage Stress (DVS) testing to screen weaker parts**
  – 1.2x ~ 1.8x stress voltage during testing
  – Failure Analysis of failed parts to seek the process improvement or spec refining

• **Statistical Yield/Bin Limit (SBL/SYL) in testing**
  – to separate the maverick parts for risk assessment
  – Maverick mechanism (yield limit by step/machine) on assembly process

• **Wafer selection rule with specific WAT risk parameters**
  – to separate marginal/risk wafer for assessment/tightened screening
Summary

• Reliability is handled throughout all stages
  – DFT, physical implementation and production
• GUC flow is based on volume production experience - allows minimal defects and very low FIT
  – Silicon-proven comprehensive DFT and testing methodology
  – Overcome challenging of 28nm/16nm DFM rules
  – Proprietary Solution for Process Variation Monitoring
  – Intelligent Mechanisms for Testing: ELFR, DVS testing, SBL/SYL and Maverick mechanism
Thank you!

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