OTP and MTP Non-Volatile Memory IP for Standard Logic CMOS Technologies

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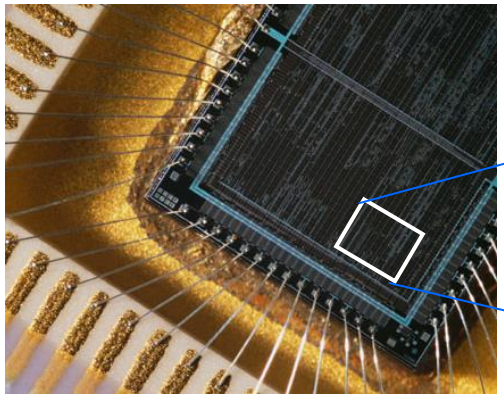
Embedded Logic OTP/MTP NVM Technology



Non-Volatile Memory IP on CMOS Process Platforms

Applications:

- **-Program Code**
- **-Security Code**
- **-Analog Trimming**
- **-SRAM Repair**
- **-Gamma Correction**

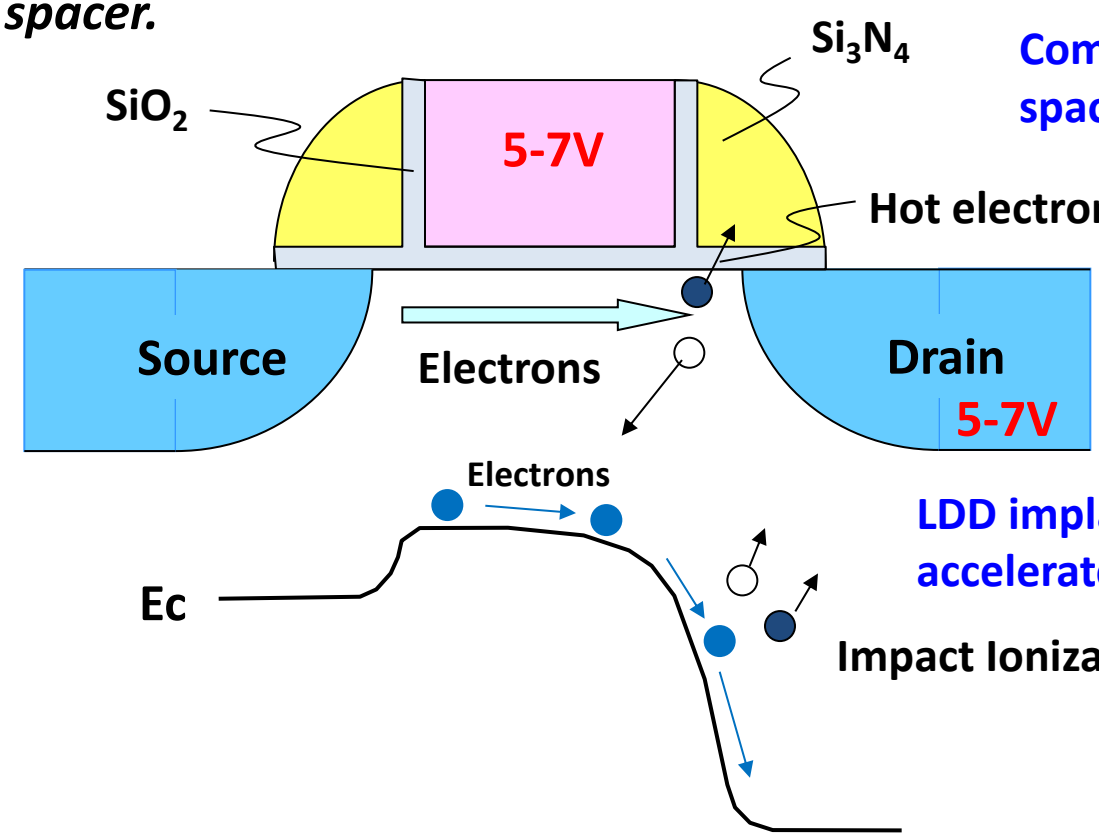
Benefits to LSI Design:

- ✓Reduced Cost
- ✓Reliability
- ✓Improved Security Level

Program, Read and Erase Mechanism

Programming Mechanism

When nMOSFET turns ON, hot-electrons are generated and trapped in side-wall spacer.

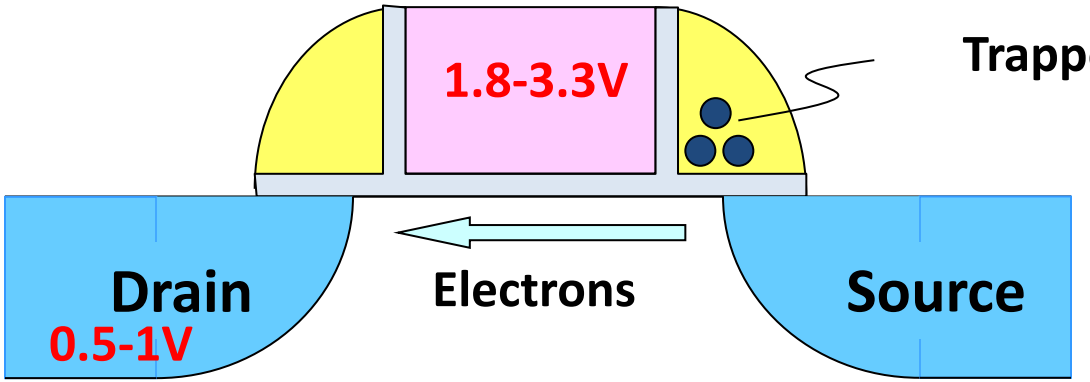


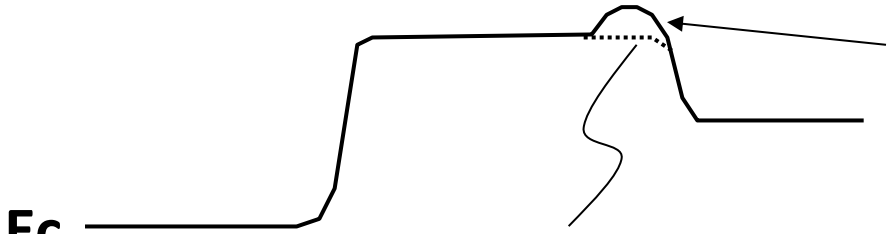
Common sidewall spacer structure

LDD implant is masked to accelerate impact ionization.

In Read Operation

"Source" and "Drain" are reversed from Program Operation



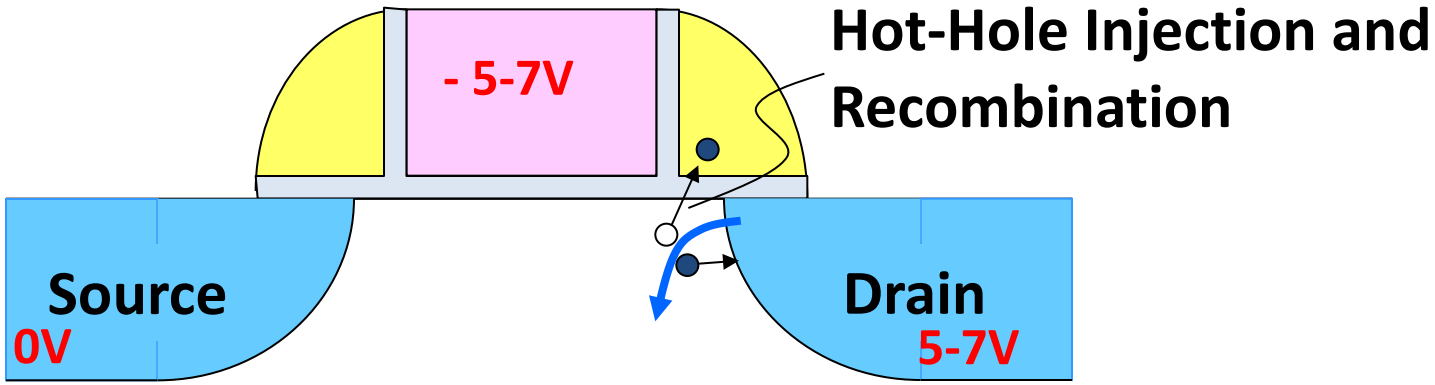


Conduction band without electron trapping

Trapped electron bends the conduction band to form a barrier.
➔ Channel current is reduced.

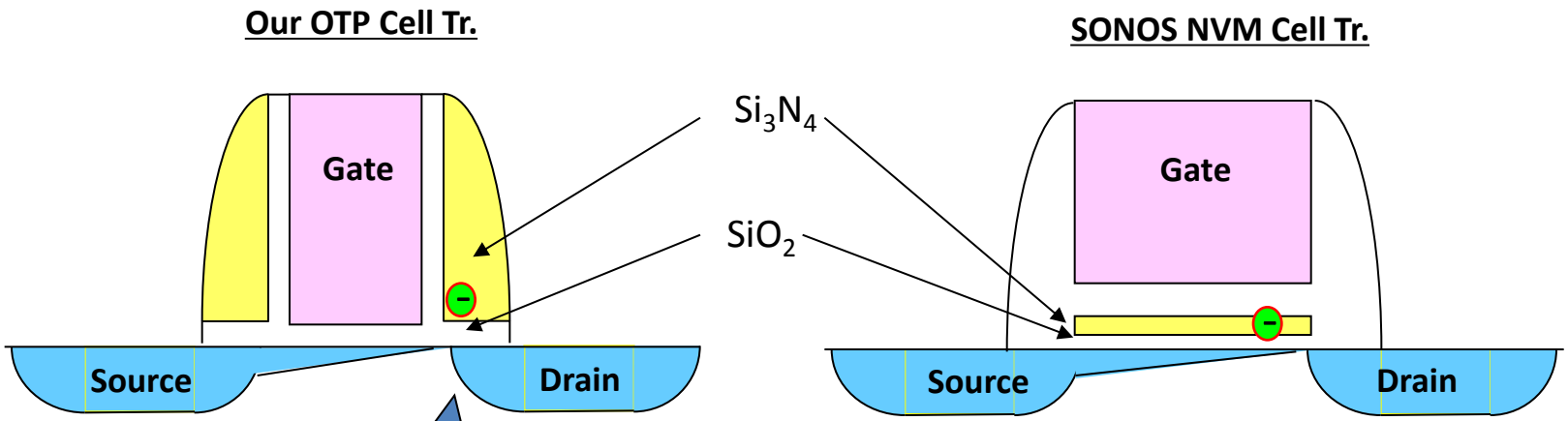
Erase Mechanism for MTP

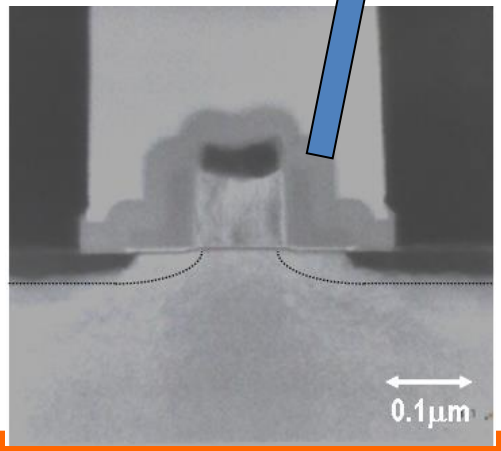
When Gate is negatively biased, hot-holes are injected into the spacer and recombine with the trapped electrons.



Band-to-Band Tunneling current generates hot-carriers.

Similarity with SONOS Memory



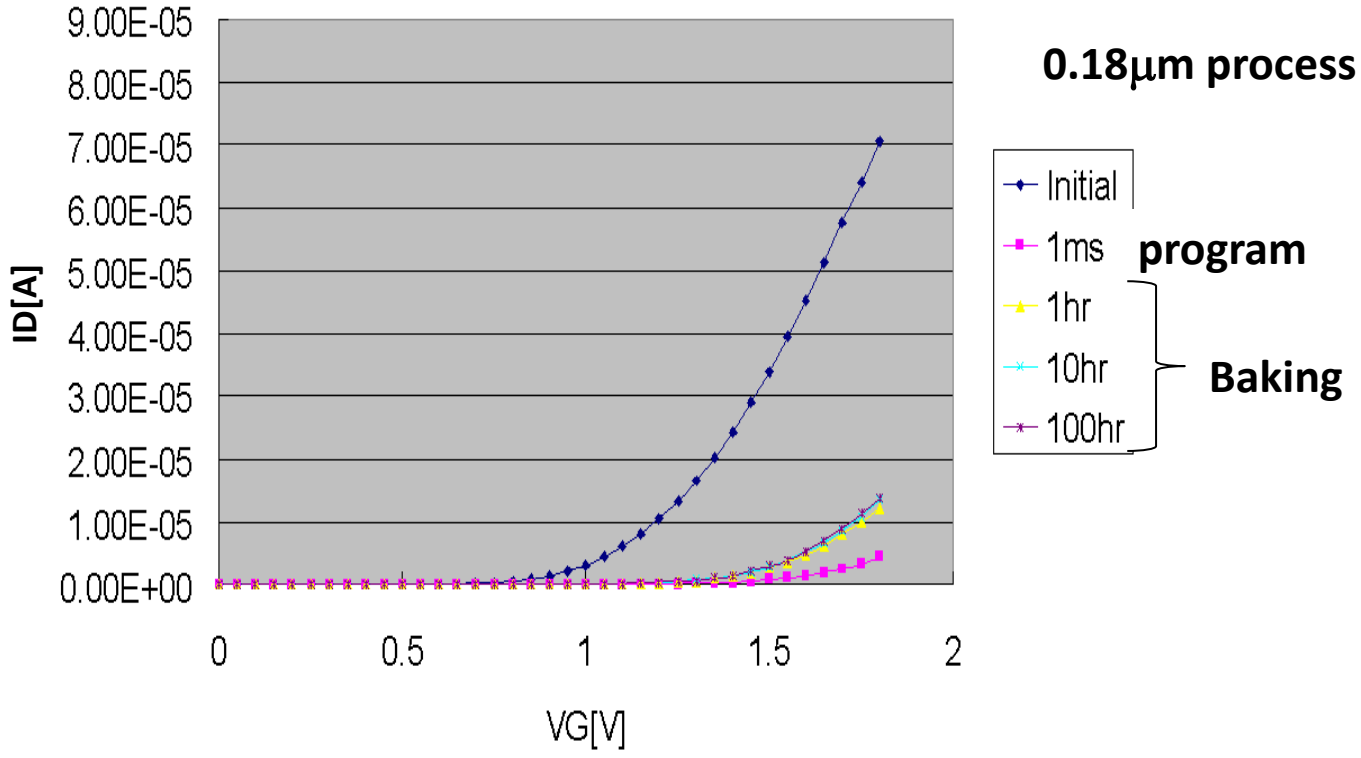


Program mechanism in Our OTP is similar to SONOS memory, which has strong track record as embedded Flash memories.

Both memories uses electron trapping in Si_3N_4 layer. Our OTP does not need any extra process, while SONOS requires special gate structure.

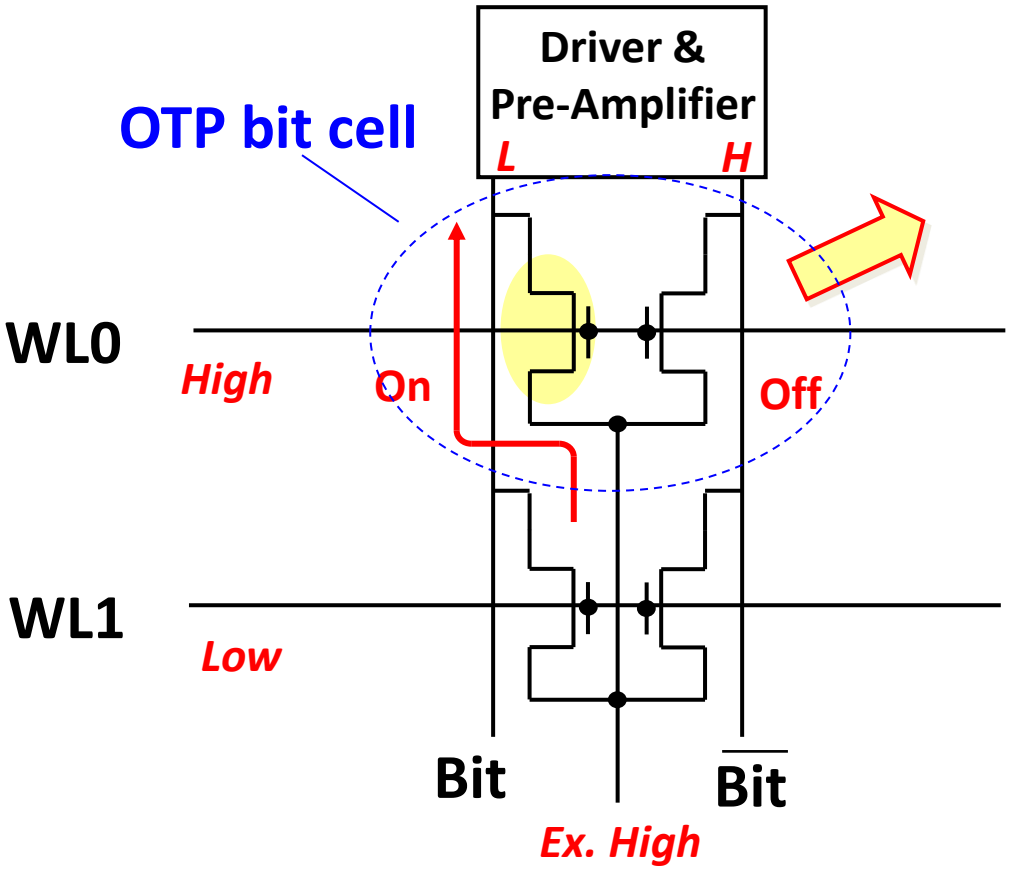
Excellent Retention Characteristics

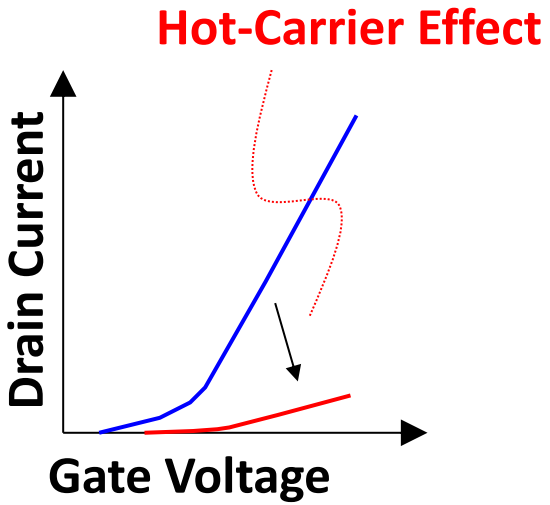
The cell current was drastically reduced and has been stable even after baking for 100 hours at 200 ℃, which is equivalent to over 30 years at 125 ℃.



Program Operation

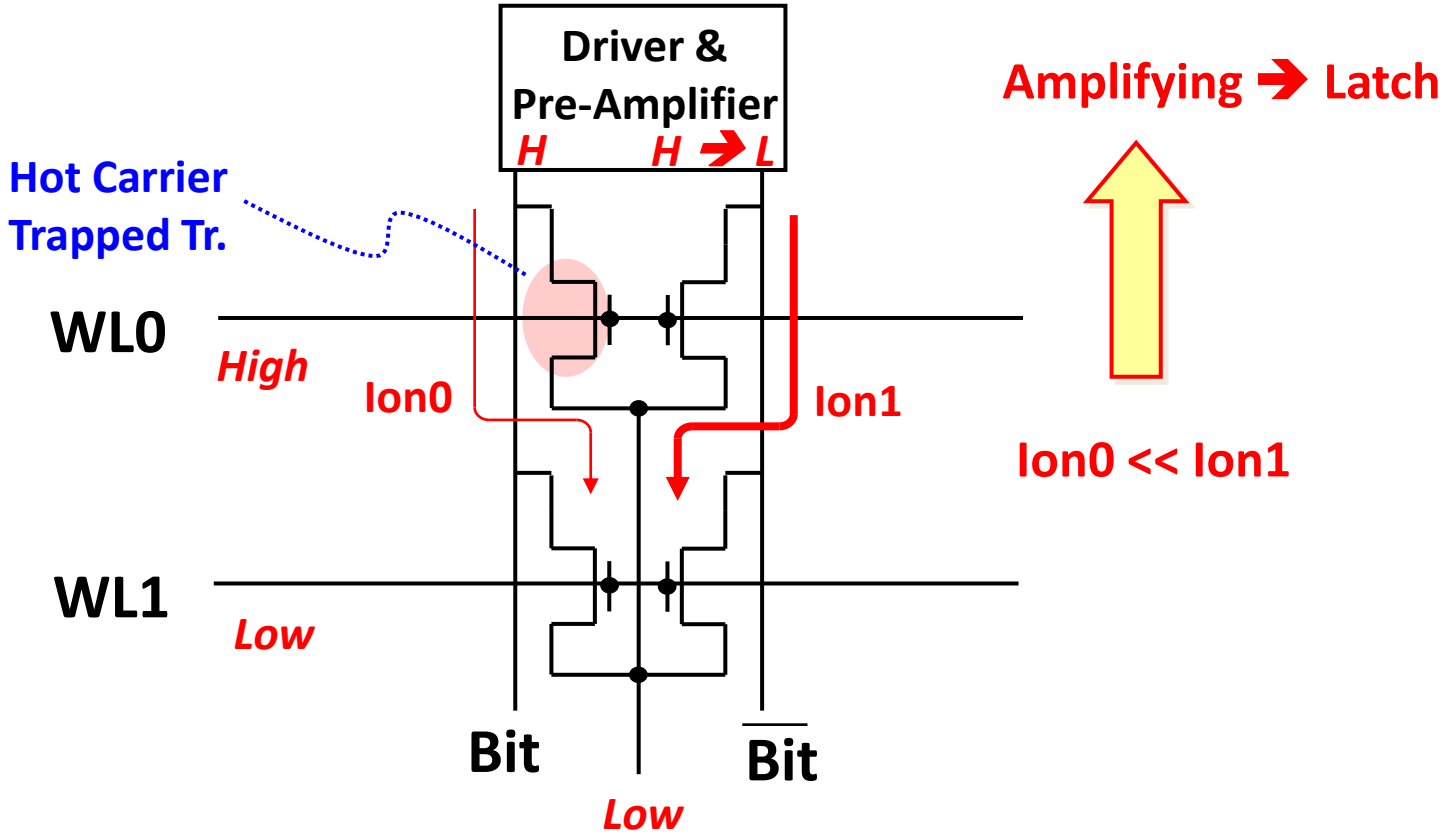
Program current flows in one transistor in a cell and generate hot-carriers.





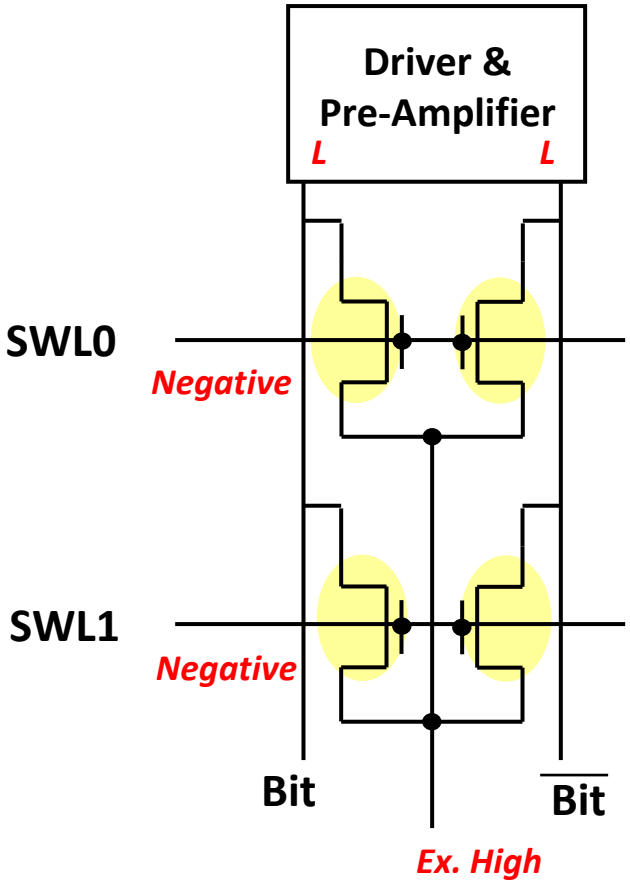
Read Operation

Both bit-lines are pre-charged and current flows through selected cell transistors.
➔ Sense amplifier senses current difference and latches.



Erase Operation for MTP

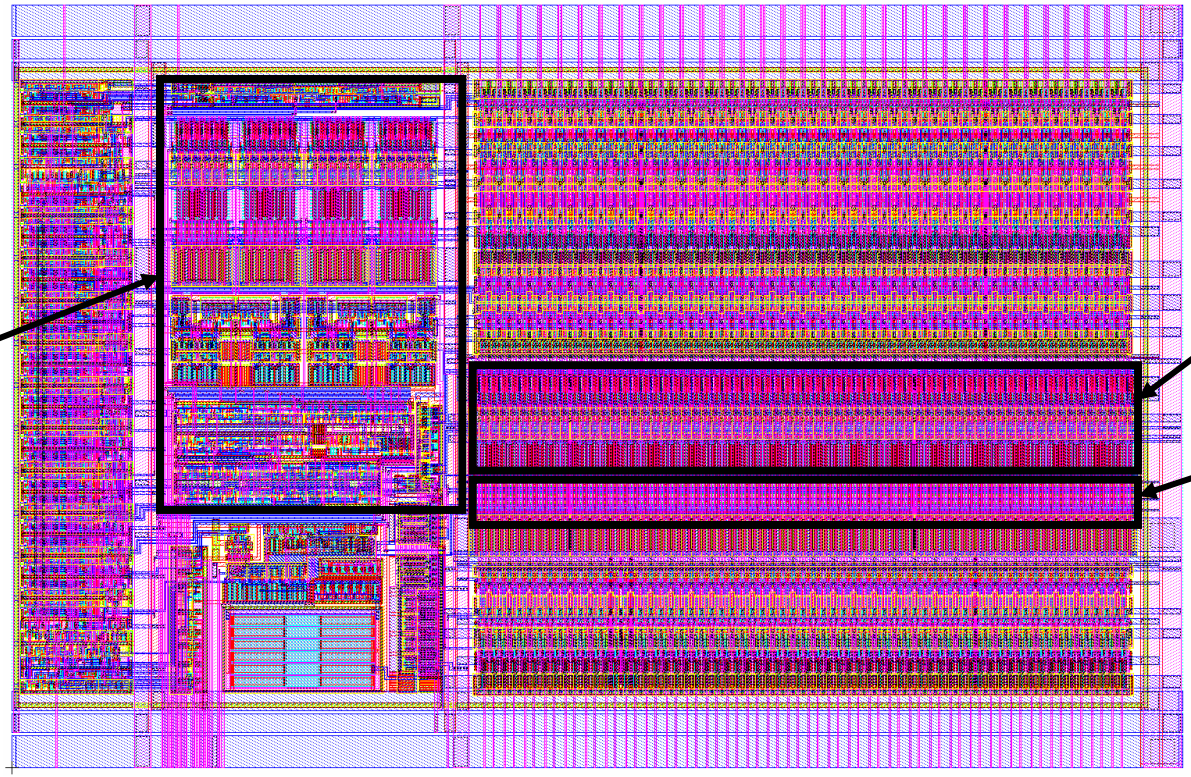
Data at all word-lines can be erased at the same time.



OTP Technology
PermSRAM™

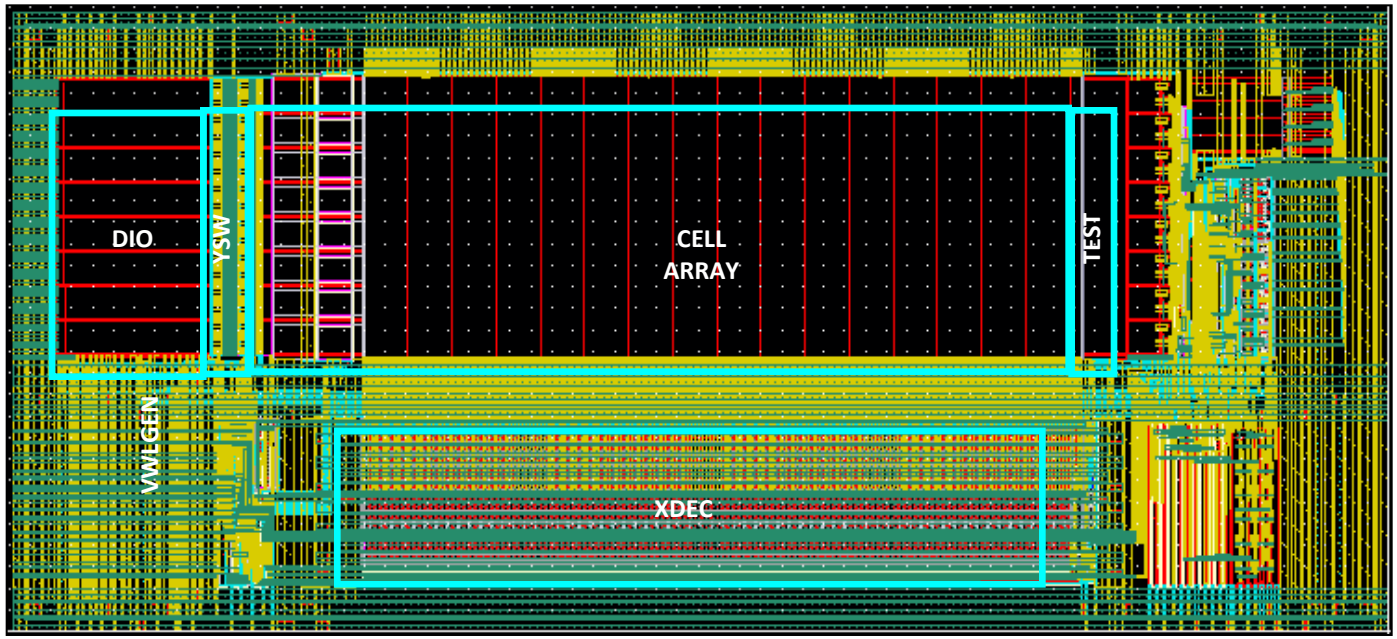
256b OTP/64b 4-Time-Programmable

-Single-Word Architecture
-Process Generation: 0.13μm Process
-IO: 64b (configurable from 1b to 256b)
-Metal Usage: 3 Layers (no limitation on routing over the macro)



16Kb One-Time-Programmable

-SRAM-Like Architecture
-Process Generation: 65nm Process
-IO: 64b
-Metal Usage: 3 Layers (no limitation on routing over the macro)



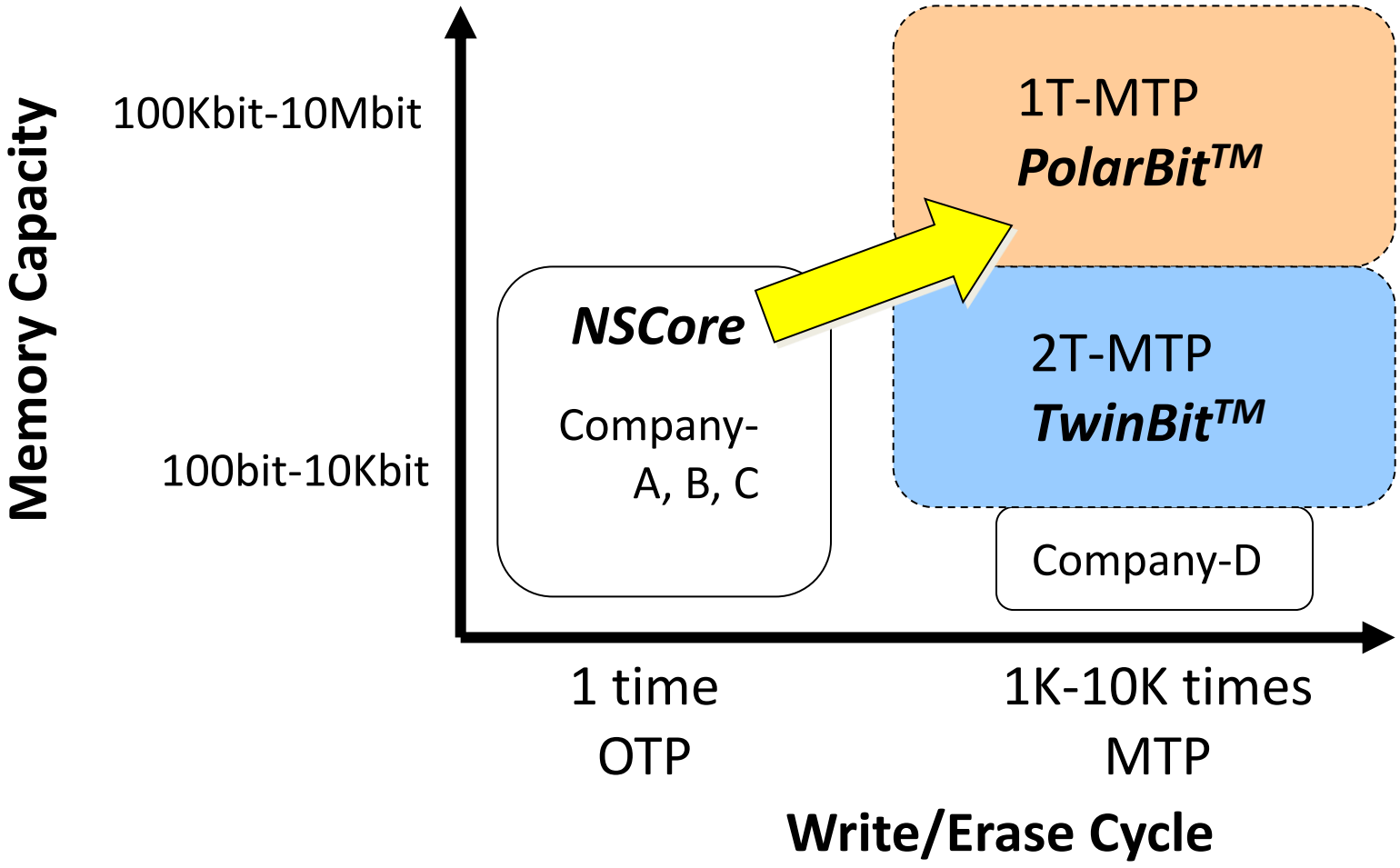
(329um x 144um)

OTP Availability in Foundry Processes

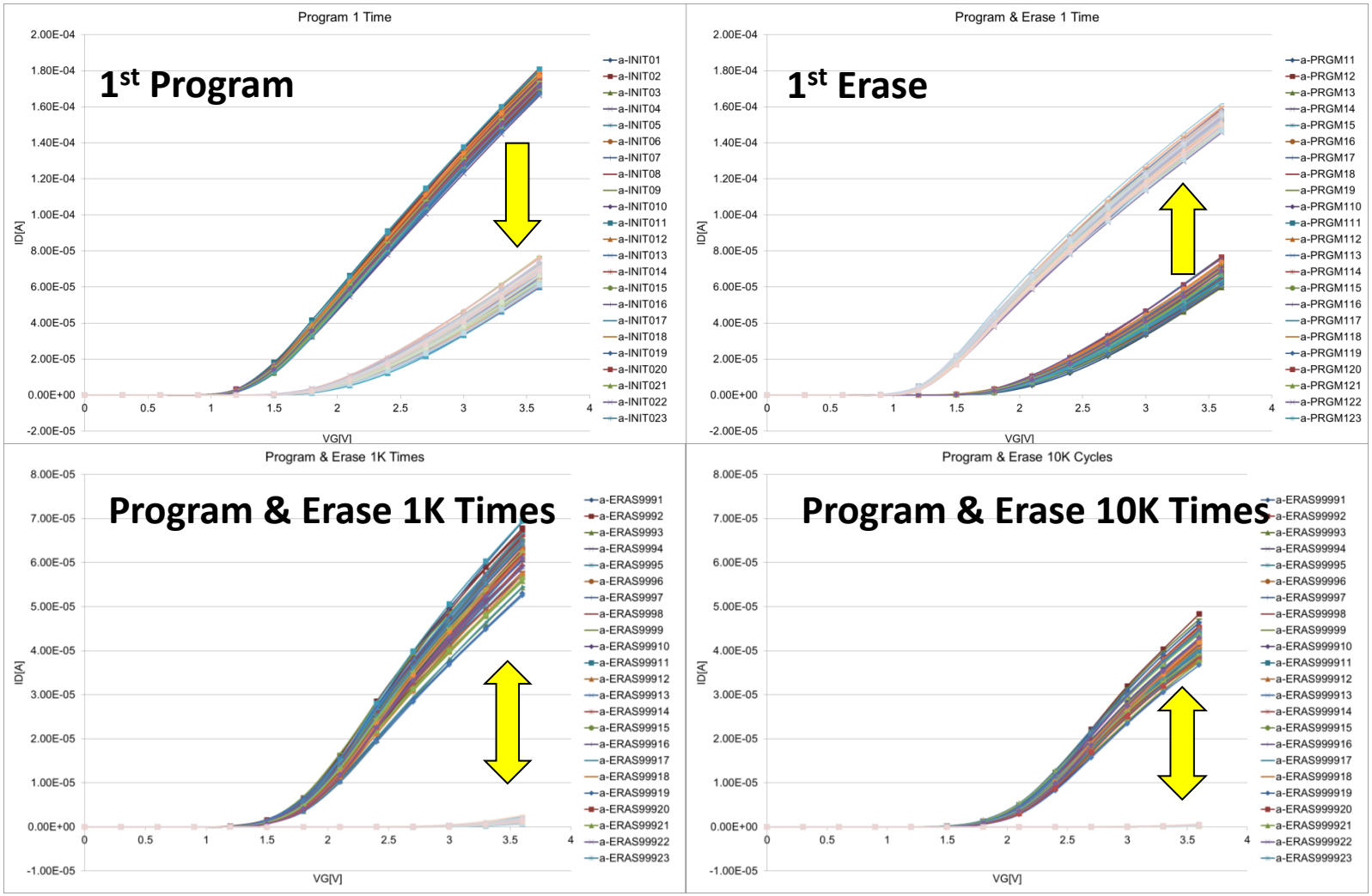
TSMC 0.18µm	***IP9000 Full Qual.,*** Volume Production
TSMC 0.13µm	***IP9000 Full Qual.,*** Volume Production
TSMC 0.11µm	Silicon Verified
TSMC 90nm	Silicon Verified
TSMC 65nm	***IP9000 Full Qual.,*** Volume Production
IBM 0.18µm	***Ready-for-IBM,*** Volume Production
TowerJazz 0.18µm	***Full Qualification***
UMC 0.11µmAE	Silicon Verified
UMC 0.11µmE	Silicon Verified
SMIC 0.13µm	Silicon Verified
GF 0.13µm	Silicon Verified
Silterra 0.18µm	Silicon Verified
Silterra 0.13µm	In Silicon Verification
Silterra 0.11µm	In Silicon Verification
LFoundry 0.15µm	In Silicon Verification
LFoundry 0.11µm	In Silicon Verification

2T-MTP Technology
TwinBit™

Targeted Market Segment of Our MTP

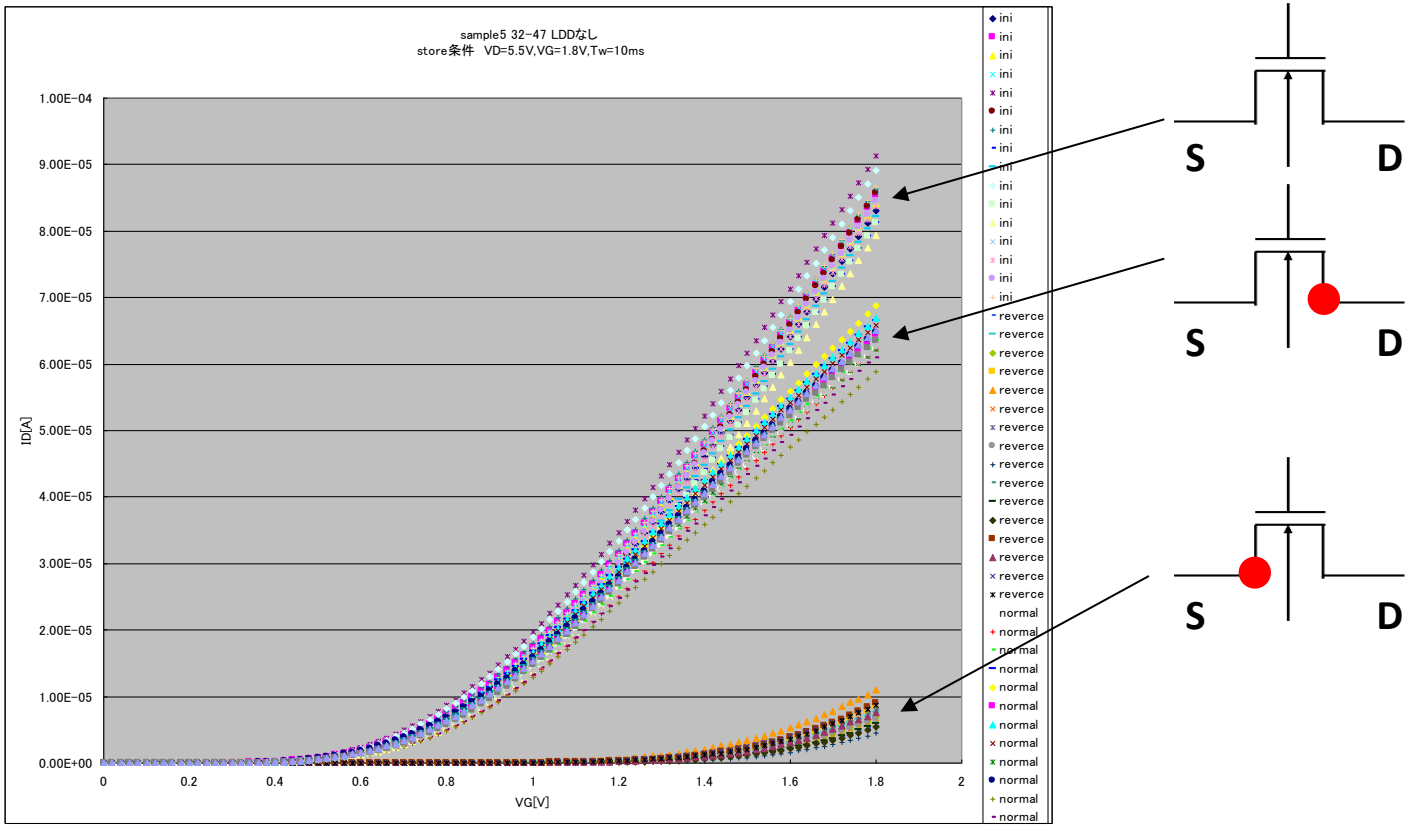


Program/Erase Characteristics



1T-MTP Technology
PolarBit™

Polarity of Vg-Id Characteristics



Technology Comparison

	NSCore's MTP "PolarBit"	Embedded Flash	Conventional CMOS MTP
Bit Area	1	2	20-100
Endurance	10K-100K cycle	1K-10K cycle	100K cycle
Add. Mask	0/+1 Mask	+10 Mask	None
Add. Process	None	Stacked Poly	None
Read Cycle	30-50MHz	30-50MHz	30MHz
Max. Operation Temp.	125-150ºC	125-150ºC	125ºC
Retention (10years@)	85-150ºC	85-150ºC	85-125ºC
Program Voltage	5.5V	10V	20V
Read	Byte	Byte	Byte
Program	Block	Block	Byte
Erase	Block	Block	Byte

Summary

✓We have developed and qualified unique OTP and MTP non-volatile technologies using hot-carrier trapping mechanism.

✓ The electron trapped in Si_4N_3 layer in the MOSFET spacer is very stable even at high temperature.

✓ We have demonstrated 10K cycle endurance and over 20 years retention at 150C for 2T-MTP.

✓ 1T-MTP has a potential to replace existing embedded Flash memory IPs.